



AEROSPACE INFORMATION REPORT

AIR6219™

Issued 2018-08
Reaffirmed 2023-07

Development of Atmospheric Neutron Single Event Effects Analysis for Use in Safety Assessments

RATIONALE

This document provides an example process for analyzing neutron Single Event Effects (SEE) for an electronic based airborne system for use in system safety assessments.

AIR6219 has been reaffirmed to comply with the SAE Five-Year Review policy.

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1. SCOPE

This document provides an example process for analyzing neutron Single Event Effects (SEE) for an electronic based airborne system for use in system safety assessments. This example has been used when the safety assessment process was in need of a SEE analysis.

1.1 Purpose

Galactic cosmic rays and solar rays penetrate the earth's atmosphere and produce particle cascades. The atmospheric radiation is comprised mainly of high energy neutrons that can interact with a semiconductor device's silicon structure causing adverse behavior.

This document describes an example process to evaluate the effects of atmospheric radiation at the equipment level, based on effects on electronic circuits. Additional atmospheric radiation information can be found in other industry documents including the IEC 62396 series. This AIR is intended to support a safety analysis; there may be other uses for this SEE analysis, but these are not specifically addressed in the document. The document is not intended to define specific data formats or organizational responsibilities. There may be other acceptable approaches to supporting SEE analyses within safety assessments.

NOTE: This document only addresses the activities that are used for equipment level SEE considerations. Benefit from system level mitigation may be used during the system safety assessment process (ARP4761/ED135). For the purposes of this document, equipment is defined as any self-contained assembly composed of one or several hardware and software items that perform a distinctive function necessary to the operation of the system.

This document primarily covers neutron effects, as they have the greatest impact on semiconductor device behavior in the atmospheric radiation environment. This document does not address the following:

- Alpha particles
- Other cosmic particles
- Electronic noise or other electronic sources of adverse behavior

1.2 Document Format

This AIR contains the following sections:

Section 1 is an introduction to the document, giving its scope and format. Also included is background information on the atmospheric environment and definitions of the resulting Single Event Effects.

Section 2 contains a list of references to other documents, definitions and acronym lists.

Section 3 describes the purpose for which the example SEE analysis process was used.

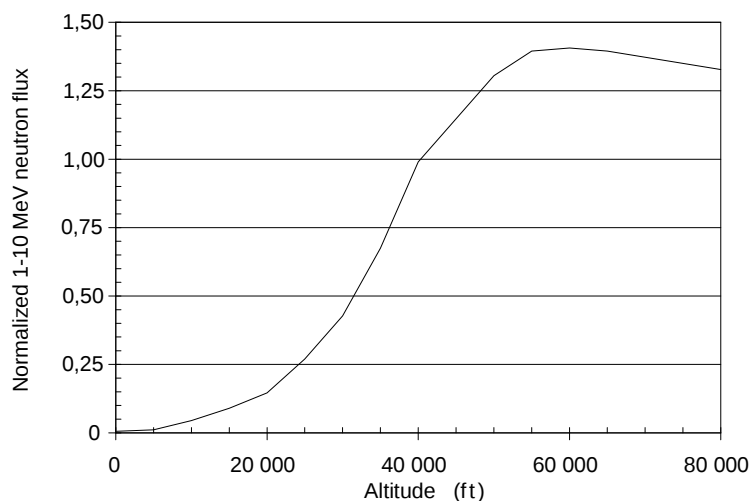
Section 4 describes the example SEE analysis process.

Section 5 provides the application of the example SEE analysis process.

1.3 Description of Atmospheric Radiation

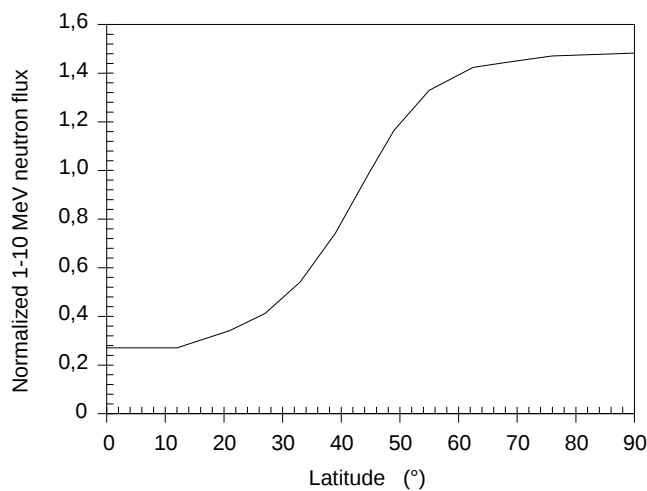
High energy primary cosmic rays continuously arrive at the Earth and interact with atoms in the Earth's atmosphere creating secondary high energy particles. Of the various secondary particles created, high energy neutrons have been shown to be the main cause of SEE in electronic aircraft devices, as reported since the early 1990s. Single Event Upsets (SEU) are one type of SEE. SEE cover a range of effect types which are all caused by a single energetic particle. The different types of SEE are described in Table 1. A full discussion of the atmospheric radiation environment is covered in detail in IEC 62396-1.

For neutrons, as well as all other secondary particles within the atmosphere, altitude, latitude, and energy are the primary parameters aiding our understanding of the SEE rate of occurrence. The result of the neutron interaction with the atmosphere is (1) a maximum flux rate at about 60000 feet; this is referred to as the Pfozter maximum, and (2) an overall variation of the neutron flux (energy range of 1 to 10 MeV) with altitude (based on aircraft measurements). Figure 1 presents the neutron flux density as it varies with altitude¹. The latitude variation of the atmospheric neutrons is governed primarily by the earth's magnetic field¹. The overall variation of the atmospheric neutron flux (energy range of 1 to 10 MeV) with latitude (based on aircraft measurements) is shown graphically in Figure 2¹.



IEC 919/12

Figure 1 - Simplified model of atmospheric neutron flux variation with altitude



IEC 921/12

Figure 2 - Simplified model of atmospheric neutron flux variation with latitude

¹ IEC 62396-1.

1.4 SEE Types

SEE are induced by the interaction of an ionizing particle with electronic components. A SEE occurs when the charge resulting from the ionization is greater than the critical charge in the component. The term SEE encompasses all of the potential effects on a semiconductor device caused by its interaction of a single particle of radiation, in this case a neutron. Table 1 provides a list of the most common SEE behaviors. IEC 62396 contains a comprehensive list of SEE types and effects.

The various types of SEE can cause a momentary or permanent change in the state of a device. Electronic hardware can be damaged, as is the case of a burn out or gate rupture, but most often the failures are non-destructive. Consideration of each applicable SEE type within a component is useful as input to the design phase, when determining mitigation techniques, and the part selection process. Note: even if non-destructive, some SEE may have an impact on system safety.

Table 1 - SEE type description and component examples

Single Event Effects	Definition	Additional Information for Device/Function Level Response
Single Event Upset (SEU)	A change of state in a bit, register or latch in a device when the radiation absorbed by the device is sufficient to change the logic state of a bit. NOTE: After a new write cycle, the original state can be recovered.	SEUs typically appear as transient pulses in logic or support circuitry, or as bit flips in memory cells or registers.
Multiple Bit Upset (MBU)	The energy deposited in the silicon of an electronic component by a single ionizing particle causes upset to more than one bit in the same word.	A MBU can cause multiple bit errors in a single word. Conventional error correcting code (ECC) schemes used in memories and caches may not correct double bit errors. MBUs have been shown to increase for smaller technologies, and recent advances in feature size have led to some components with MBU rates that are comparable to SEU rates. Interleaving may provide protection.
Multiple Cell Upset (MCU)	A single event that induces two or more bits in an Integrated Circuit (IC) to upset at the same time. NOTE: The error bits are usually, but not always, physically adjacent.	MCUs can affect a large number of cells. The errors in an MCU tend to be physically close and therefore it is likely that they affect more than one bit of the same memory word, which could be classified as an MBU. Interleaving may provide protection.
Single Event Latchup (SEL)	The triggering of a parasitic PNP circuit in bulk CMOS, resulting in a state where the parasitic latched current exceeds the holding current. This state is maintained while power is applied. The condition is caused by an increase in current due to a regenerative current flow condition which activates the device. Both high current and low current SELs can occur. Low current latchups will still require power cycling but will not damage the component.	Latchup can cause circuit lockup and/or device failure. May or may not cause permanent failure but requires power cycling to return IC to normal operations if undamaged.

Single Event Effects	Definition	Additional Information for Device/Function Level Response
Single Event Transient (SET)	Spurious signal or voltage induced by the deposition of charge by a single particle that can propagate through the circuit path during one clock cycle.	Produces transients which may affect subsequent circuits if not well filtered in the design. Examples include transients on external signals for comparators, and internal transients for CMOS devices leading to erroneous data. NOTE: For frequencies above 100 MHz the potential for SET in digital devices increases.
Single Event Functional Interrupt (SEFI)	The occurrence of an event, usually in a complex device (e.g., microprocessors, modern memory components, complex power management components, FPGAs, etc.) such that a control path is corrupted, leading the part to cease to function properly.	A single event effect in a complex device such that a control path is corrupted, leading to a temporal loss of device functionality. Often induced from an SEU in the control registers of a complex device and recovered by reset or power cycle. NOTE: This effect has sometimes been referred to as lockup, indicating in which case the device is put into a "frozen" state.
Single Event Gate Rupture (SEGR)	Occurs in the gate of a powered insulated gate component when the radiation charge absorbed by the device is sufficient to cause gate rupture, which is destructive. An SEGR is manifested by an increase in gate leakage current and can result in either the degradation or the complete failure of the device.	Devices which may be susceptible include: power MOSFETs, non-volatile NMOS structures, large integrate devices, and linear devices.
Single Event Burnout (SEB)	The burn out of a powered electronic component or part thereof as a result of the energy absorption triggered by an individual radiation event.	A condition which causes device destruction due to a high current state in a power semiconductor device. Power MOSFETs are most susceptible.
Single Event Hard Error (SHE)	Hard errors in devices such as memory, take the form of "stuck" bits. The error is "hard" because the device no longer functions properly, even after power reset and re-initialization.	A SHE causes a change to the operation of a device which may persist over multiple flight cycles. The device may no longer meet its performance expectations as the same bit remains incorrect after re-write cycles. Error detection and correction (EDAC) may provide a solution.

1.5 Independence and Probabilistic Nature of SEE

Due to the random nature of atmospheric neutron energy at a particular device location and the highly localized nature of SEE, the resulting events are considered independent from each other, and SEE rates are estimated probabilistically.

1.6 Consideration of Extreme Space Weather

The sun can influence the neutron flux within the atmosphere in two main ways: (1) the impact of solar activity on the intensity of galactic cosmic rays reaching earth and, (2) occasional extreme space weather events which can result in large bursts of solar particles arriving in the atmosphere, creating a short increase in the atmospheric neutron flux.

During periods of high solar activity (e.g., solar flares) the flux density may rise to a level significantly higher than that normally experienced. The flux density utilized for design analysis purposes is based on average levels determined by the airframer and as this includes occasional periods of extreme space weather events, further consideration in this respect is not necessary.

No consideration is provided for rare solar events that might significantly increase neutron flux for short periods (hours to days). During these events, the faults would continue to be random (i.e., not a Common Mode). These events are outside the scope of this example.

The protection and mitigation incorporated into airborne electronic systems based on the normal levels of atmospheric radiation will also provide some protection and mitigation for the extreme solar and cosmic radiation event environments. Further information regarding extreme space weather can be found in the following report: *Extreme Space Weather – Impacts on Engineered Systems and Infrastructure. Royal Academy of Engineering – February 2013* and *EASA Safety Information Bulletin SIB No. 2012-09 Effects of Space Weather*.

1.7 Thermal Neutrons

There is an additional SEE rate in some devices contributed by very low energy neutrons (called thermal neutrons). While the high energy neutrons cause SEE through interaction with the Si atoms, thermal neutrons cause SEE through their interaction with Boron-10 that is found in some microelectronics. Parts containing Boron-10 or natural boron are typically avoided when possible. When assessing SEE rates, thermal neutron effects may be considered when appropriate; information can be found in 5.6 of IEC 62396-1 and in IEC 62396-5.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this document to the extent specified herein. The latest issue of SAE publications shall apply. The applicable issue of other publications shall be the issue in effect on the date of the purchase order. In the event of conflict between the text of this document and references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2.1.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606- 7323 (inside USA and Canada) or +1 724-776-4970 (outside USA), www.sae.org.

ARP4761 Guidelines and Methods for Conducting the Safety Assessment Process on Civil Airborne Systems and Equipment

2.1.2 EUROCAE Publications

Available from EUROCAE Secretariat, 102 rue Etienne Dolet, 92240 Malakoff, France, Tel: +33 1 40 92 79 30, www.eurocae.net.

ED135 Guidelines and Methods for Conducting the Safety Assessment Process on Civil Airborne Systems and Equipment

2.1.3 IEC Publications

Available from IEC Central Office, 3 rue de Varembe, P.O. Box 131, CH-1211 Geneva 20, Switzerland, Tel: +41 22 919 02 11, www.iec.ch.

IEC 62396-1 Process Management for Avionics – Atmospheric Radiation Effects – Part 1: Accommodation of atmospheric radiation effects via single event effects within avionics electronic equipment (2016) Note: Section 7 should not be applied in support of the ARP4761.

IEC 62396-2 Process Management for Avionics – Atmospheric Radiation Effects – Guidelines for single event effects testing for avionics systems (2012)

IEC 62396-3 Process Management for Avionics – Atmospheric Radiation Effects – Guidelines to optimize avionics system design to reduce single event effects rates (2013)

- IEC 62396-4 Process Management for Avionics – Atmospheric Radiation Effects – Guidelines for designing with high voltage aircraft electronics and potential single event effects (2013)
- IEC 62396-5 Process Management for Avionics – Atmospheric Radiation Effects – Guidelines for assessing thermal neutron fluxes and effects in avionics systems (2013)

2.1.4 EASA Publications

Available from European Aviation Safety Agency, Ottoplatz, 1, D-50679 Cologne, Germany, Tel: +49 221 8999 000, www.easa.europa.eu.

EASA Certification Memorandum – EASA CM No.: EASA CM – AS – 004 Issue: 01 issued 08 January 2018. Single Event Effects (SEE) Caused by Atmospheric Radiation.

EASA Safety Information Bulletin SIB No. 2012-09 and Cert Memo

2.2 Other References

EIA JEDEC JESD 89A (2006) Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices

EIA JEDEC JESD 89-3 (2005) Test Method for Beam Accelerated Soft Error Rate

2.3 Definitions

This section provides definitions for unique terms used in this document. Citations are provided to other industry sources when usage in this document is consistent with the definition in the referenced source material.

CROSS-SECTION (σ): A combination of sensitive area in the component and probability of an interaction depositing the critical charge for a SEE. The cross-section may be calculated using the following formula: $\sigma = \text{number of errors/particle fluence}$. The units for cross-section are cm^2 per semiconductor device or cm^2 per bit.

EQUIPMENT: For this document, any self-contained assembly composed of one or several items that perform a distinctive function necessary to the operation of the system.

FIT: Failures in time. For SEE 1 FIT equals one event per $1\text{E}9$ device hours.

INTERLEAVING: By interleaving memory, logically adjacent bits are physically separated.

SINGLE EVENT EFFECT: Response of a semiconductor device caused by the impact of a single particle (e.g., galactic cosmic rays, solar energetic particles, energetic neutrons and protons).

SEE TYPE: A unique semiconductor device behavior, identified as being related to an atmospheric radiation event.

2.4 Acronym List

ADC	Analog to Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
ECC	Error Correcting Code
EIA	Electronic Industries Alliance
EDAC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable Read Only Memory

FET	Field-Effect Transistor
FIT	Failure In Time
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
IEC	International Electrotechnical Commission
JEDEC	Joint Electron Device Engineering Council
LET	Linear Energy Transfer
MBU	Multiple Bit Upset
MCU	Multiple Cell Upset
MeV	Million electron Volts
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
PLD	Programmable Logic Device
N	Neutron
NMOS	N-type Metal-Oxide-Semiconductor
PSSA	Preliminary System Safety Assessment
RAM	Random Access Memory
SEB	Single Event Burnout
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SHE	Single Event Hard Error
SEL	Single Event Latchup
SEU	Single Event Upset
SER	Soft Error Rate
SET	Single Event Transient
SOI	Silicon On Insulator
SRAM	Static Random-Access Memory
SSA	System Safety Assessment
TLB	Translation Lookaside Buffer

3. PURPOSE OF SEE ANALYSIS PROCESS

The purpose of a SEE analysis process is to evaluate the electronic circuits utilized in a particular design for their sensitivity and response to neutron radiation. This sensitivity and response information are used during the development phase to evaluate SEE impact on safety assessments, including integrity and availability requirements.

4. EXAMPLE SEE ANALYSIS PROCESS

This section describes a method to assess the potential contribution of atmospheric radiation effects, as an aspect of the overall system safety assessment process. This contribution could be used together with the other safety aspects addressed by ARP4761/ED135 processes.

Figure 3 outlines the steps involved in a SEE analysis process that includes both qualitative and quantitative phases. From the parts list, sensitive devices are identified. The SEE analysis determines SEE rates and evaluates internal device mitigations. In addition, the SEE analysis may also determine the effect of any mitigations at the equipment level. If the results of a SEE analysis indicate SEE rates to be unacceptably high, testing can be performed to address unacceptable effects or rates, or a decision for a design change can be made. A design change can include a parts selection change, or additional mitigation. When the evaluation is complete, SEE rates are typically summarized.

All potentially susceptible components would follow the SEE analysis process. The high-level steps associated with this SEE analysis process include:

1. Prepare SEE analysis and verify process inputs.
2. Identify SEE sensitive semiconductor devices, and sensitivities within those devices.
3. Determine device mitigations and equipment effects.
4. For components needing further investigation, determine cross-section rates for each applicable SEE type.
5. Test or change design if necessary.
6. Summarize SEE rate.

4.1 SEE Preparation Phase

The preparation phase collects the operational definitions, available safety requirements, architecture and design data for use in the SEE analysis. The analysis can be performed without specific safety requirements or architecture information when determining SEE rates at the device level only.

The parts list, schematics and equipment design material are necessary to perform the parts assessment, mitigation evaluation, and cross-section definition.

4.1.1 Requirements Definition

The SEE preparation phase begins with a review of the inputs useful in performing the atmospheric radiation evaluation. The following information is used to perform the SEE Analysis:

1. Target SEE rates (e.g., a rate based on the margin of the safety requirements which can be reasonably assigned to SEE, taking into consideration random hardware failure rate estimates).
2. Neutron Flux as defined by customer, or conservative average mission based on industry standards.

The mission profile will normally be defined for the aircraft and will include the operating flight envelope of the aircraft.

The nominal neutron flux at any operational location, can be determined by scaling the nominal 6000 neutrons (n)/cm² per hour at 40000 feet altitude 45 degrees latitude, using the tables in Annex D of IEC 62396-1, as referenced in Figure 1 and Figure 2.

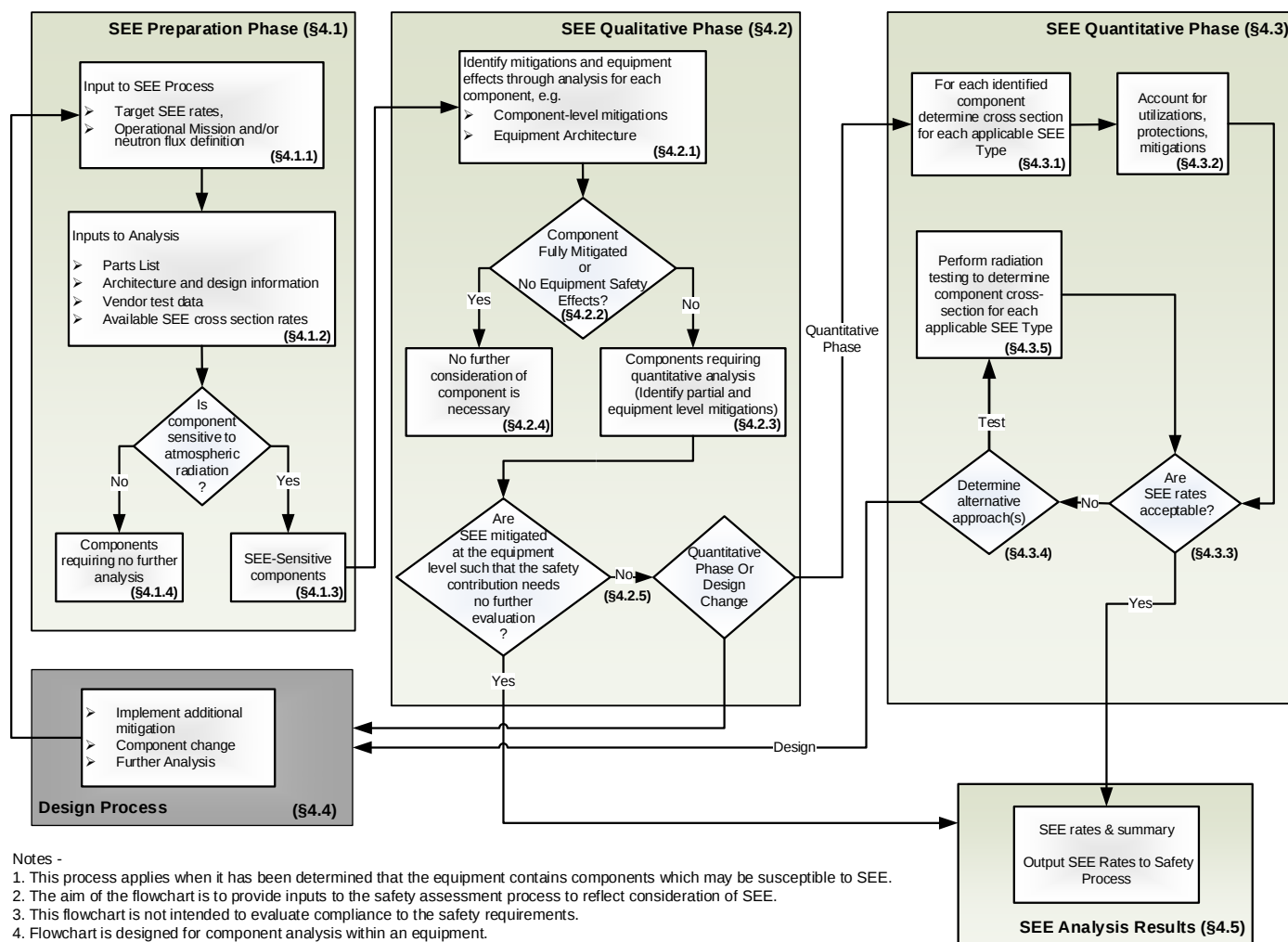


Figure 3 - Example SEE analysis process diagram

4.1.2 Inputs to Analysis

In order to perform the SEE rate analysis, data on each of the potentially SEE sensitive semiconductor devices is compiled.

The following data sources potentially offer useful SEE information:

1. Existing available component SEE test data.
2. Other supplier/vendor information on semiconductor device sensitivity and SEE cross-section rates.
3. IC device datasheets and reference manuals which may include information such as register counts.
4. Published literature.
5. IEC 62396 standard series or other industry sources of information on SEE sensitivity to atmospheric radiation.

4.1.3 Identify SEE Sensitive Components

The next step in the preparation process is to separate all of the semiconductor devices in the parts list into two groups; those that do not need to be considered further and those that are SEE sensitive. All semiconductor devices that cannot be identified as immune or having a high degree of immunity are considered to be SEE sensitive. Table 2 reflects one format able to capture this initial information; this example table could be adjusted to support individual analyses needs.

As a result of an appreciable amount of electronics industry SEE testing, conducted by exposing semiconductor devices to high energy neutrons, it is known that certain classes of semiconductor devices are sensitive to SEE. These include, but are not limited to, (a) memories, (b) microprocessors, microcontrollers and digital signal processors, and (c) field programmable gate arrays (FPGAs). The design complexity of the ICs may also be taken into account when determining if a device is SEE sensitive. For instance, there may be implementation specific details, such as control logic and registers, which can result in the occurrence of Single Event Functional Interrupts (SEFIs).

In general, as technology trends continue to achieve higher densities and lower operating voltages, semiconductor devices are becoming more sensitive to atmospheric radiation (e.g., bit upsets (SEU, MCU, and MBU) and resets (SEFIs) are some likely effects to be experienced).

Components with feature sizes greater than 1µm are less likely to be susceptible to atmospheric radiation, while components with feature sizes less than 1 µm may need to be considered for SEE. Sensitivity to SEE generally becomes greater as the feature size decreases on a per device basis.

NOTE: High voltage (>200 V) semiconductors may be sensitive to transients and burnout and may also be considered for SEE analysis, refer to IEC 62396-4.

Other SEE, such as SEL and SET, are also considered when determining the susceptibility of a device.

NOTE: The ability of SET to propagate and cause an effect increases as the clock frequency increases.

Several key pieces of information to be considered when investigating each component include:

1. The geometric feature size of the technology. Generally, for susceptible technologies, as the feature size decreases the susceptibility to radiation increases.
2. The most recent applicable component design and technology information from the manufacturer. Changes within the technology may render existing radiation test data obsolete. For example, a non-sensitive component becomes sensitive due to shrink evolution. Also, a device made by the same manufacturer and of similar form, fit and function may not necessarily exhibit the same SEE susceptibility between an older and newer version of that device.
3. A preliminary analysis using “conservative rates” may help to identify where mitigation and test data may be needed to meet safety requirements.
4. Future component changes, which may affect the susceptibility of the component, may be taken into account in the initial design and addressed with appropriate mitigations.

4.1.4 Identify Components Needing No Further Analysis

A SEE analysis is carried out on those semiconductor components that have potential for interacting with atmospheric radiation resulting in SEE. Identifying semiconductor devices which require no further analysis is completed in this step of the preparation phase. Semiconductor devices which are included in this list are categorized as either immune, shown to have no SEE rates, or SEE rates low enough as to not require further consideration. Supporting rationale may be captured.

Examples of such candidates include:

1. Passive components (those requiring no supply voltage) may be considered immune to SEE and need no further analysis.
2. Devices where an identical part was tested with high energy neutrons and no SEE resulted.
3. Devices where an identical part was tested with heavy ions and the Linear Energy Transfer (LET) threshold was greater than 15 MeV-cm²/mg, and no SEL resulted. The results of heavy ion testing have shown good correlation with the atmospheric neutron environment for latch ups.
4. The SEE rates for the component are at least an order of magnitude lower than the random hardware failure rate of the device for the same failure mode, and therefore may have an insignificant contribution to the safety analysis results.
5. Older non-volatile memories, for example EEPROM and Flash memories with feature sizes greater than 250 nm, have generally been considered SEE immune. However, devices with smaller feature sizes have been shown to have a sensitivity to atmospheric neutron radiation.
6. Example factors to evaluate when a sensitive component may not contribute in an appreciable numerical way include:
 - Total number of bits within component which may be sensitive to atmospheric radiation
 - Percent utilization rates
 - Operational mission factors

The electronic components listed in this section represent those that have been identified as being effectively immune to SEE (or have an insignificantly low level of sensitivity to SEE). Such components may need no further consideration in a SEE analysis. Test references and rationale are captured as applicable for non-passive components. Table 3 shows an example method of capturing this information along with the supporting rationale.

Table 3 - Example List of semiconductor devices requiring no further analysis

Generic Part #	Company Part #	Semiconductor Device	Vendor	Rationale for SEE immunity	Supporting information
XXY	BBXX	Op-Amp		Test data verifies no SEE	
XXZ	NAAA	Voltage Regulator		Data indicates SEE rate is not an appreciable numerical factor	

4.2 SEE Qualitative Phase

The qualitative phase reviews existing mitigations against SEE and the effectiveness of those mitigations. This phase may also take into account equipment safety effects if provided from the safety process. Available SEE data from the preparation phase is utilized during the qualitative phase to complete a review of the component's SEE sensitivity. This phase of the SEE analysis applies to SEE sensitive components. The resulting mitigation may remove the need to perform quantitative analysis for the component being considered.

Mitigation can be employed at the component, equipment, or system level. Not all SEE which propagate through an equipment result in a failure. For example, if a fault occurs in an unused part of the equipment, no effect occurs. Those faults that do propagate through the equipment may result in detected or undetected failures or may have no effect.

Detected failures may result in application termination, application correction, or memory bit correction. A consequence of undetected failures may be silent data corruption.

4.2.1 Identification of Mitigations and Equipment Effects

A qualitative assessment is performed for the remaining components which were not eliminated by the actions in 4.1. These components are reviewed to determine whether internal device mitigations against SEE exist, and any remaining device sensitivities that are not covered by the internal mitigations are identified for equipment level consideration. Determination of the effectiveness of a component level mitigation is based on the component and equipment level effects.

Note, when reviewing mitigations that include device utilization percentages, conservative assumptions may be made in terms of the device utilization percentage, such that future increases in utilization percentage are unlikely to have an impact on the safety assessment. Equipment level mitigations and architecture design considerations may be identified and taken into account at this stage, or later during the system safety process.

4.2.2 Component Mitigation and Equipment Effects Decision

With component level mitigations identified, determine if the device is fully mitigated or if any unmitigated sensitivities can result in a safety effect.

When reviewing a component, all of the various functions within the device are assessed and all applicable SEE types are identified. For example, if EDAC is utilized for a memory device, SEUs would be addressed for the memory bits, and if interleaving is employed, MBUs may also be mitigated. However, the control function of the memory device may still be susceptible to SEFIs.

If, for each function, all applicable SEE has been mitigated, then the component can be considered fully mitigated. Any remaining un-mitigated SEE, on a per function basis, need to be accounted for in an analysis. For those components not fully mitigated, determine if the effect of unmitigated sensitivities can result in a safety effect. If the analyst is able to confirm that such unmitigated sensitivities are incapable of contributing to a compromise in aircraft safety, then quantitative analysis may not be necessary for the component under consideration.

Once the component mitigations are identified and a determination is made on whether or not there is an equipment level safety effect, a determination can be made as to the need for a quantitative assessment for each susceptible component.

Examples of Functions with Component Mitigation include:

- Power electronic circuits can be designed to operate successfully in radiation environments. Design considerations include selecting and applying components, including circuit topology and voltage derating, to survive in a radiation environment. For example, a component which has a latch up sensitivity, but only when powered at maximum voltage, can be considered as fully mitigated for SEE by ensuring the device power supply voltage is limited.
- Triple Modular Redundancy is a mitigation technique which includes a voting capability to address a SEE in any one path of the circuit. The redundancy can be specifically added for critical data or to perform data calculations. This design option can be implemented in hardware or software. The design would include the capability to clear the effect in a timely manner to mitigate against multiple single event effects. Rates for both SEUs and MBUs would be addressed when implementing this mitigation.

Example of Functions with "No Safety Effect" include:

- Maintenance logging function: the logging function gathers information about the specific equipment but plays no part in the functioning of the equipment in normal flight operation. Faults in the component or logging function will have no effect on the safe operation of the equipment.
- Test port: functions and associated components which are not utilized during operation and are proven incapable of causing an effect, and therefore have no safety effect.

4.2.3 Identify Components Requiring Quantitative Analysis

If the semiconductor device is not fully mitigated and could also impact the safety of the equipment, then identify any partial mitigations and supporting data. These components require further analysis as described in the Quantitative Phase.

4.2.4 List of Components Exempt from Quantitative Analysis

Those devices which are fully mitigated or produce no resulting equipment safety effects due to SEE require no further investigation. The analysis can apply at the semiconductor device, or equipment level. Perform this analysis for each instance of a sensitive component within the equipment. The component along with the mitigations and supporting data is captured.

4.2.5 Component Mitigation Determination and Decision for Design Change or Quantitative Phase

After all SEE sensitive components have been evaluated, a determination is made as to the need for further analysis. If further analysis is needed, a decision is made whether to perform a quantitative analysis (4.3) or consider a design change (4.4). This evaluation takes into account all available SEE information, component and equipment level mitigations and equipment safety effects. If the SEE which are un-mitigated at the equipment level, result in failure conditions that are being evaluated by safety that are classified as minor or lower, no further evaluation may be needed.

4.3 SEE Quantitative Phase

A quantitative assessment is performed for the SEE sensitive components where remaining unmitigated SEE could result in Safety effects.

4.3.1 Calculate Component/Bit Type Cross Sections

For those semiconductor devices being evaluated quantitatively, the SEE cross-section for each bit type is determined. For the components with partial mitigation, the analysis is performed on the un-mitigated portion(s). The device cross-section is a measurement of the device/bit susceptibility to radiation; it is defined as the ratio of the number of upsets to the particle fluence. This provides a way of adjusting the probability that the semiconductor will interact with neutrons based on the flux density based on operational mission parameters and allows calculation of the probability that the semiconductor will interact with neutrons and results in a SEE rate.

4.3.1.1 Identify Available SEE Cross Sections

The cross-section data for each bit type can be obtained for SEE susceptible components. If no data is available, conservative estimates may be used. Conservative cross-sections tend to result in high rates but can be useful in identifying where mitigations or testing would be needed. Cross-section information is captured; e.g., incorporated into the example Table 2.

There are a number of ways to obtain cross-section data, including but not limited to:

1. Appropriate vendor information.
2. Device level SEE testing, (e.g., high energy neutron beam test).
3. Industry information including IEC 62396 as a source which provides information about conservative cross-sections for some components (see below for specific sections of the IEC containing this information).

IEC 62396 contains guidance on conservative SEE cross-sections for some types of integrated circuits. This guidance is mainly in the form of SEE cross-section data plots. The referenced document lists the various types of SEE atmospheric neutron cross-sections and addresses some of the limitations in compiling that SEE cross-section data. Feature size is one of the most relevant integrated circuit technology parameters influencing variation of SEE cross-section. The guidance is based on assembling published SEE cross-section data to observe how the cross-sections vary with the feature size. However, as seen in some of the data plots, there can be variations of 1 to 2 orders of magnitude in the cross-sections.

Issues with obtaining SEE Cross-Section Data:

- Many reports in publicly available literature with SEE data do not name the specific devices.
- SEE response in many publicly available references can be hidden by expressing it in relative terms (that is arbitrary units) and for upsets with units of FIT or FIT/Mbit; however, the latter can be converted to a cross-section in units of cm^2/bit by using the conversion factor $7.1\text{E-}17 \text{ Mbit-cm}^2/(\text{FIT-bit})$ which is based on a neutron flux ($E > 10 \text{ MeV}$) of $13 \text{ n/cm}^2\text{hr}$ at New York City (refer to JESD 89A).
- SEU, MCU, and MBU are often expressed on a per bit basis, while SEFI rates are often expressed on a per device basis.
- Access and availability of test facilities.

4.3.1.2 SEE Rate Calculation Methods

Testing provides the most accurate means of establishing SEE cross-sections. Note that of the possible options available for establishing cross-sections, testing yields the least conservative cross-section rates. Changes to the device, such as die shrink or manufacturing location, can invalidate the test results and require retest or the use of conservative rates.

Testing generally results in cross-section measurements with units of " cm^2/bit " for SEU, MCU, and MBU. For other effects including SEL, SEFI, and SEB, the effect may need to be based on the response of the entire semiconductor device such that the units are " $\text{cm}^2/\text{device}$ ". For example, because the number of memory bits in a RAM device are known, the SEU rates would be provided on a per bit basis. However, for the SEFI rate of a microprocessor, where the total number of registers is not provided by the manufacturer, the units would be expressed on a per device basis.

The simplified method of calculating the nominal SEE rate for a particular SEE type is to multiply the SEE cross-section for that type (units of cm^2) by the integrated neutron flux; for example, 6000 n/cm^2 per hour (Energy $> 10 \text{ MeV}$) [IEC 62396-1]. When calculating SEE rates for devices with smaller geometries, which may be impacted by lower energy neutrons, the neutron flux with energy between 1 and 10 MeV is added to the 6000 n/cm^2 per hour, as shown below. [Refer to Section 8 of IEC 62396-1.] The 6000 n/cm^2 per hour flux (Energy $> 10 \text{ MeV}$) is a nominal value for 40000 feet (12.2 km) altitude and 45 N latitude and may be scaled for different altitudes and latitudes.

Examples of SEE rate calculations:

SEE rate per bit hour = $[6000(\text{n/cm}^2 \text{ per hour}) + (1\text{-}10\text{MeV rate if applicable})] \times \text{SEE cross-section } (\text{cm}^2 \text{ per bit})$

Or

SEE rate per device hour = $[6000(\text{n/cm}^2 \text{ per hour}) + (1\text{-}10\text{MeV rate if applicable})] \times \text{SEE cross-section } (\text{cm}^2 \text{ per device})$

The analyst may capture a description of the sources and assumptions needed to obtain the tabulated cross-section values. For example, the basis for the similarity between the device being analyzed and the device with test data is justified only under certain conditions (e.g., same manufacturing process by same IC vendor, same feature size, same fab). Guidance for these assumptions can be found in IEC 62396-1, Annex B and Annex G and IEC 62396-2 as well as reviews of published data.

4.3.2 Account for Device Utilizations, Protections, Mitigations

Once the cross-section is determined, the SEE impact can be determined by taking into account device and equipment level utilizations, protections and mitigations. This analysis can go beyond the component level mitigations and take into account whether or not there is a safety effect, as described in 4.2.2, and include mitigations/protections/architecture at the equipment level. Table 2 provides an example of how this could be documented. This evaluation addresses each bit type within a component and the associated SEE type(s).

SEE rates can be adjusted for the conditions used within the design. This includes the number of bits/registers utilized, on-chip mitigation and equipment level mitigation. Mitigations are not effective unless they are fast enough to catch the event before a failure condition can be realized.

Examples of mitigations/protections against SEE include:

1. Device/bit utilizations

- a. Include only the bits utilized in the design
- b. Account for the total number of control registers in components such as FPGAs

2. Timing aspects

- a. Active monitors
- b. Watchdog timer and bit-stream CRC
- c. Results checking, data range limits, and input data filtering to address transients

3. Component level mitigations

- a. Triple modular redundancy
- b. Interleaving design
- c. On chip EDAC

4. Equipment level mitigations

- a. Data scrubbing; error correction technique which uses a background task that periodically inspects memory for errors
- b. Voting
- c. Lockstep architecture
- d. EDAC and parity checking
- e. Triple modular redundancy; hardware or software
- f. Data reasonableness monitoring

5. Protections

- a. Filters, exposure window, data range-checking, continuous monitoring and exception handling, watchdog supervisory logic, error correction, and partitioning.

NOTE: Automatic initiated resets may lead to system availability dropouts and may need to be considered against availability requirements in the safety analysis. For example, in case of SEFI or other SEE generating equipment fault, automatic initiated resets and/or power resets may lead to system availability dropouts.

4.3.3 Determine if SEE Rate is Acceptable

The decision on whether or not a SEE rate is acceptable can be made on either a component basis, or cumulative component basis. After the SEE rates have been calculated using the available component cross-sections, device utilizations, protections, and mitigations determine if the resulting SEE rate will be acceptable. At this point ensure that all assumptions are acceptable.

If the SEE rate is not within the range of the equipment safety requirements, a decision is made as to next steps. The options available are defined in the following two sections.

4.3.4 Determine Alternative Approach(s)

When the quantitative assessment indicates an unacceptably high probability that the component could be affected by SEE, compared to the safety requirements, the following options may be considered:

1. Architecture re-design to include additional mitigation(s) (4.4).
2. Re-design of the component or use of a different component (e.g., different specification or technology) (4.4).
3. Radiation testing of the component to determine a less conservative SEE rate (4.3.5).

4.3.5 Perform Testing

When the quantitative assessment indicates an unacceptably high probability that the component could be affected by SEE, and a re-design of the component (or use of a different component) or an architecture re-design to include additional mitigation(s) is not desired, then radiation testing may be an alternative. Radiation testing is a means of obtaining accurate component cross-section data. The availability of accurate test data enables the analyst to avoid overly conservative cross-section data obtained from sources other than testing. It is considered that such techniques may reveal the acceptability of a particular component, which may then allow the design to meet its requirements without design changes. Additional information on radiation testing methods can be found in JEDEC 89 Standards.

If the radiation testing results still indicate an unacceptably high component SEE rate then an equipment redesign, or use of different component(s), may need to be considered.

4.4 Design Change

A design change can be selection of a different component, or a re-design to include additional mitigation(s). With the possibility of a new component selection, the process would begin again for that particular component at the preparation phase. If additional mitigations are incorporated, the process would begin at the qualitative phase.

Consider a design change when any of the following apply:

1. The qualitative evaluation suggests that additional SEE mitigations are needed to support achieving the safety requirements.
2. The quantitative assessment indicates safety requirements would not be achievable.

4.5 Output SEE Effect Rates to Safety Process

The semiconductor component SEE rates are documented for susceptible components including documentation of why specific components are excluded. The information developed as a result of completing the SEE analysis can be utilized as input to the safety assessment. The purpose of performing the SEE analysis is to ensure that equipment effects have been considered, thereby reducing the un-mitigated SEE rates that would need to be considered in the safety assessment.

4.6 Equipment Change Impact

Review of equipment and component changes during the life cycle of the equipment provide updates to SEE susceptibility information. This includes a review of changes to the component level SEE sensitivity, equipment design and mitigation changes. The SEE impact of a change to a component can be evaluated in a manner similar to the initial SEE evaluation.

5. SINGLE EVENT EFFECTS ANALYSIS EXAMPLE

This section continues the example by illustrating its use with example components, showing results to be utilized as input into a PSSA or SSA. The purpose of the example is to illustrate the concepts described in Section 4; it is not intended to illustrate a comprehensive list of all types of SEE sensitive devices, and therefore only a select number of components are analyzed as part of the example. In practice, the assumptions in the example may not occur but are meant for demonstration purposes only.

Figure 4 provides detailed block diagrams of example Monitor 1 and Command 1 functions. This example covers the analysis of a single fault per SEE. This example is not intended to specify a format for documentation of SEE analysis.

This SEE analysis example does not cover all aspects of a complete evaluation; among the SEE analysis characteristics not covered are:

1. Utilization of existing flight data for component rate analysis.
2. Every possible SEE susceptible component.

Figure 5 illustrates how this example maps to the Example SEE Analysis Process flowchart of Figure 3. The example steps through each phase of the process starting with the preparation phase, followed by the qualitative and quantitative phases and finishing with the SEE effects rates summarized and made available for use by the overall safety process. The SEE analysis example assesses the susceptibility of a number of selected components to radiation, evaluates mitigations, and provides a SEE rates summary. Note: As stated above, this example does not include every type of susceptible component.

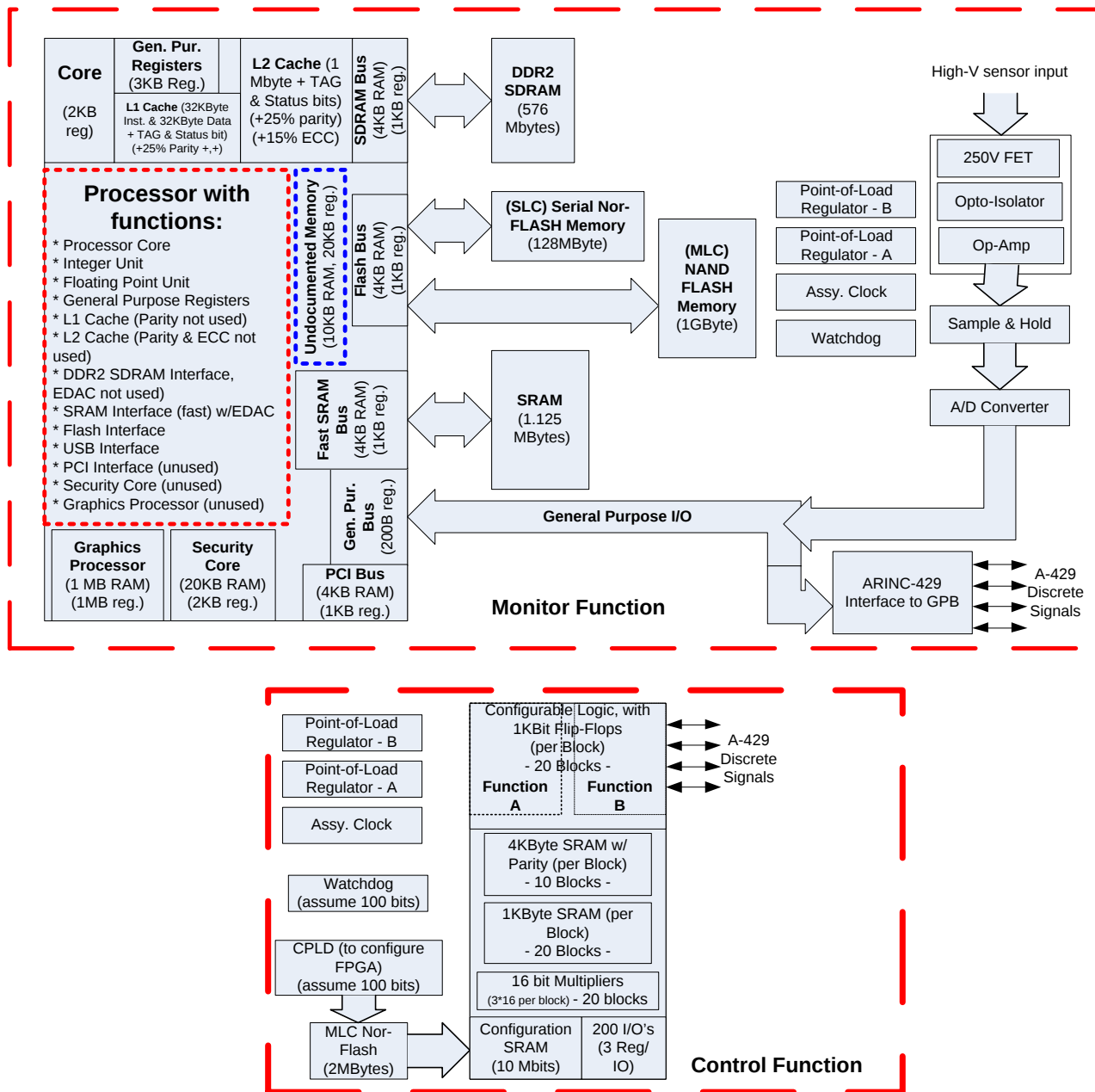


Figure 4 - SEE analysis example - Command 1 and Monitor 1 functions

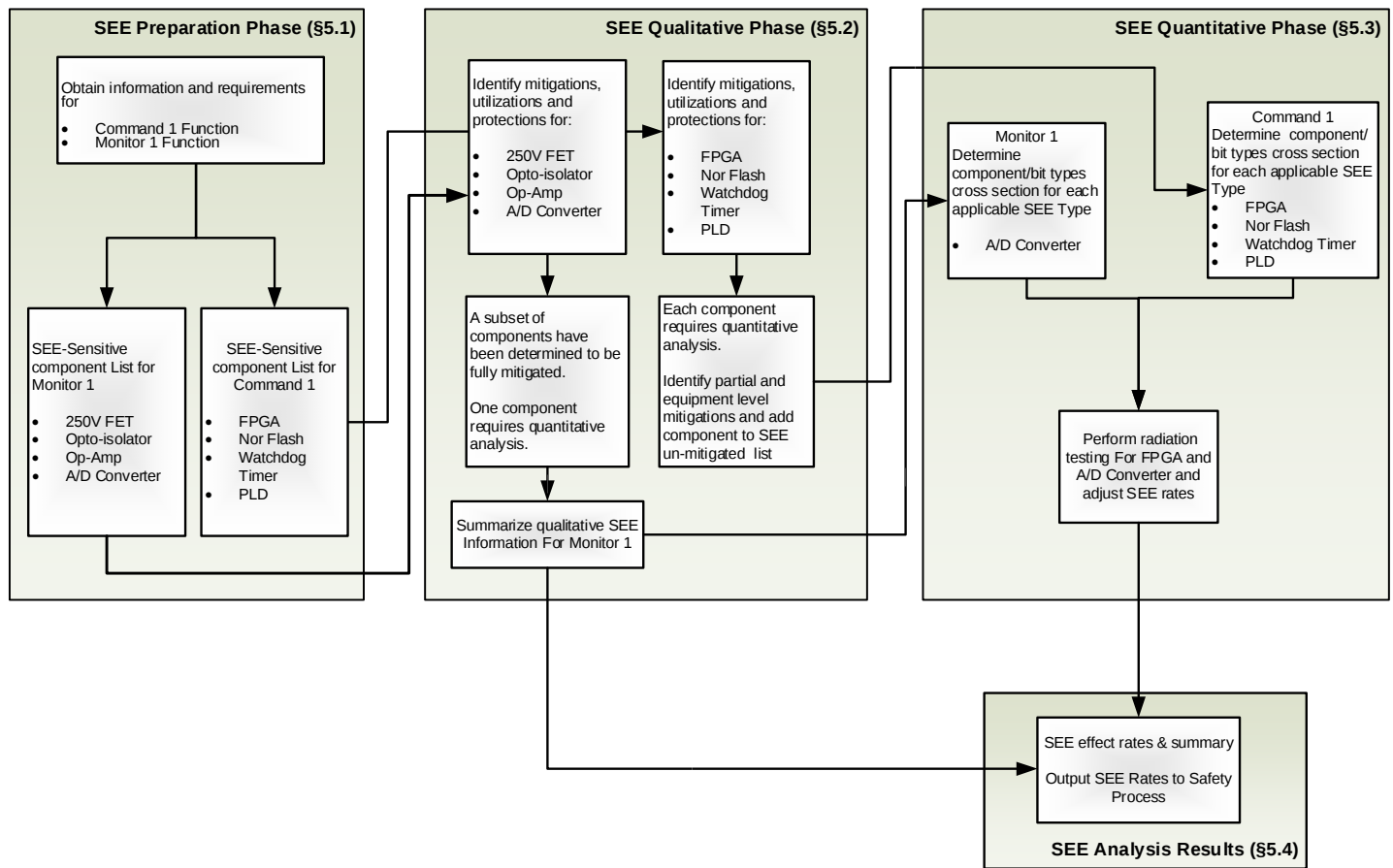


Figure 5 - Flow chart for example SEE analysis

5.1 SEE Preparation Phase for Command 1 and Monitor 1 Functions

For the SEE Preparation Phase, the design and requirements for Command 1 and Monitor 1 sub-functions were obtained. Shown below are the tables of SEE sensitive components from the Command 1 and Monitor 1 parts lists.

Table 4 and Table 5 list the components analyzed in this example, and whether or not test data is available to be used in starting the SEE analysis. The information obtained during this step will be utilized in the Qualitative Phase.

Table 4 - Monitor 1 SEE sensitive devices

Monitor 1 SEE Sensitive Devices	SEE Information
FET	No data
Opto Isolator	No data
Op Amp	No data
ADC	No data

Table 5 - Command 1 SEE sensitive devices

Command 1 SEE Sensitive Devices	SEE Information
FPGA	Only SEL data available
Nor Flash	Test data
Watchdog Timer	Test data
PLD	No data

5.2 Qualitative Phase

The qualitative phase involves determining the availability of mitigations against SEE and the effectiveness of these mitigations. Each component is reviewed to determine what mitigations exist.

5.2.1 Monitor 1 Qualitative Analysis

A qualitative analysis on the Monitor sub-function is performed. Table 6 lists the mitigations for the selected components in the Monitor 1 sub-function. For each component, the applicable mitigation is identified, and the level of mitigation is analyzed. If no or only partial mitigations apply further analysis is necessary. Based on this qualitative analysis, one of the components identified in Table 6 requires quantitative analysis.

Table 6 - Monitor 1 component evaluation

Device	Mitigations/Evaluation
250V FET	De-rating by design margin
Opto Isolator	Not sensitive in this environment due to large feature size
Op Amp	SOI design; this technology is proven to be less susceptible to radiation
ADC	No data available

5.2.2 Command 1 Qualitative Analysis

A qualitative analysis on the Command sub-function is performed. Table 7 lists the mitigations for the selected components in the Command 1 sub-function. For each component, the applicable mitigation is identified, and the level of mitigation coverage is analyzed. If no or only partial mitigations apply further analysis is performed. Each function within a complex device is reviewed separately for all applicable SEE. Based on this qualitative analysis, each of the components identified in Table 7 requires quantitative analysis.

Table 7 - Command 1 component evaluation

Device	Mitigations/Evaluation
FPGA	SRAM employs on-chip EDAC. 34 Kbits SRAM with design utilizing 15.6%. NVM is not utilized in design therefore no Quantitative analysis is needed. 100% utilization assumed for registers. SEFI rates apply. SEL test data available.
Nor-Flash	2 Mbytes Nor-Flash holds 10 Mbit FPGA initial configuration. The 10 Mbit includes the initial state of all SRAM arrays. Use of internal registers is ignored. A CRC is employed, and configuration is normally performed on the ground. This single point of failure would not cause a failure in flight.
PLD	10 of 200 registers are utilized in design.
Watchdog Timer	SEL test data available.

5.3 Quantitative Phase

A quantitative assessment is performed for the remaining components in both sub-functions, where no mitigation or only partial mitigation was identified.

5.3.1 Monitor 1 Quantitative Analysis

A quantitative assessment is performed on the ADC device as no data is available. This component is identified as a test candidate. For the purpose of this example, a neutron flux rate (based on 40000 feet and 45 N Latitude) of 6000 N/cm² per hour is utilized. To conclude this quantitative analysis, the Component Sensitivities and Evaluation sections of the SEE Analysis Table are completed. Each function within a complex device is analyzed separately and all types of applicable SEE rates are provided. Table 8 provides the Quantitative Analysis results for the Monitor 1 sub-function.

Table 8 - Monitor 1 SEE analysis table

Monitor 1 equipment example component SEE sensitivities								Evaluation				
Manufacturer Part #	Ref. Design	Device Type	Description/ Feature Size (nm)	SEE Sensitivity Description with on-chip mitigations	Total # Potential bits prone to SEE	SEE cross-section (cm ² /bit)	SEE cross-section (cm ² /device)	Neutron Flux utilized in calculation	BOM Quantity	Utilizations (%)	Mitigations/Protections	Final SEE Rate (error/hour)
		250V FET	NA	SEB rates apply	per device rate applies	NA	1.00E-14	6000	1	100%	Derating of the device	0.00E+00
		Opto Isolator	300	SET, SEL rates apply	per device rate applies	NA	6.50E-08	6000	1	100%	R/C filtering mitigates transients. By normal operations latchup would be cleared.	0.00E+00
		Op Amp	NA	SET, SEL rates apply	per device rate applies	NA	1.60E-11	6000	1	100%	1. SOI technology not latch up sensitive. 2. R/C filtering mitigates transients.	0.00E+00
		ADC	130	SET, SEL, SEFI rates apply	per device rate applies	NA	1.50E-11	6000	1	0%	No mitigations	9.00E-08

5.3.2 Command 1 Quantitative Analysis

Table 9 provides a review of the available data, and mitigations identified in the qualitative phase. The FPGA is a test candidate. This example does not provide details on the test development, experiment and test data analysis. For the remainder of the example, the rates utilized will be the completed test results.

Table 9 - Command 1 quantitative evaluation

Device	Component SEE Data
FPGA	Only SEL test data is available. FPGA is a test candidate as the conservative rates would result in an unacceptable SEE rate for the various functions within the component. Data to be updated based on test results. Note: On-chip EDAC mitigation can be justified because it is fast enough to prevent detect/correct before reading failure condition.
Nor-Flash	Test Data Available, utilized selected device.
PLD	Utilize IEC62396-1 Annex G conservative rates, utilized selected device.
Watchdog Timer	Utilization factors taken into account. SEL test data available.

For the purpose of this example, a quantitative analysis is performed on each of the selected components. SEE cross-section rates, a neutron flux rate (based on 40000 feet and 45 N Latitude) of 6000 n/cm² per hour, and all application mitigations are utilized in this analysis. To conclude this quantitative analysis, the Component Sensitivities and Evaluation sections of the SEE Analysis Table are completed. Each function within a complex device is analyzed separately and all types of applicable SEE rates are provided. Table 10 provides the Quantitative Analysis results for the Command 1 sub-function.

Table 10 - Command 1 SEE analysis table

Command 1 equipment example component SEE sensitivities								Evaluation				
Manufacturer Part #	Ref. Desig.	Device Type	Description/ Feature Size (nm)	SEE Sensitivity Description with on-chip mitigations	Total # Potential bits prone to SEE	SEE cross-section (cm ² /bit)	SEE cross-section (cm ² /device)	Neutron Flux utilized in calculation	BOM Quantity	Utilizations (%)	Mitigations/Protections	Final SEE Rate (error/hour)
		FPGA	65	uSRAM - SEU	34,816	1.76E-14	6.13E-10	6000	1	15.6	Utilization factors for memory cells.	5.73E-07
				uSRAM - MBU	34,816	9.27E-15	3.23E-10	6000	1	15.6	Utilization factors for memory cells.	3.02E-07
				Registers - SEU	8,192	1.26E-14	1.03E-10	6000	1	100	--	6.18E-07
				Registers - MBU	8,192	2.32E-14	1.90E-10	6000	1	100	--	1.14E-06
				SEFI	1	--	1.90E-10	6000	1	100	--	1.14E-06
				SEL	1	--	0.00E+00	6000	1	100	Test Data	0.00E+00
		Nor Flash	90	Nor-Flash 2MByte	16,777,216	1.00E-18	1.68E-11	6000	1	62.5	1. Utilization factors for memory cells.	6.29E-08
				Registers	1,000	1.00E-18	1.68E-11	6000	1	0	1. CRC used for internal registers.	0.00E+00
		Watchdog Timer	120	SET - Registers	10	1.00E-12	1.00E-11	6000	1	50	Utilization factors for device.	3.00E-08
				SEFI per Device	1	--	1.00E-10	6000	1	100	--	6.00E-07
				SEL per Device	1	--	0.00E+00	6000	1	100	Test Data	0.00E+00
		PLD	150	Control Registers Only (IEC 62396 Annex G)	200	1.00E-11	2.00E-09	6000	1	5	10 bits are utilized in design.	6.00E-07

5.4 SEE Analysis Results

For the Command 1 and Monitor 1 sub-functions, the SEE rates and summary information are compiled and made available for use within the overall safety process. For this example, both the qualitative and quantitative rates for the subsystems are provided, to be used as input to a safety assessment.

6. NOTES

6.1 Revision Indicator

A change bar (|) located in the left margin is for the convenience of the user in locating areas where technical revisions, not editorial changes, have been made to the previous issue of this document. An (R) symbol to the left of the document title indicates a complete revision of the document, including technical revisions. Change bars and (R) are not used in original publications, nor in documents that contain editorial changes only.

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